(1) (a) What’s the function of the translation lookaside buffer (TLB)? (2%)
(b) Please describe the relationship between “TLB miss” and “page fault”. (4%)
(c) As shown in Fig. 1, there are two points to perform the TLB lookup; one is before the cache access (as Design_A), and the other is after the cache access (as Design_B). What are the advantages and disadvantages of the Design_A and Design_B? (6%)

(2) (a) Please define the temporal locality and spatial locality. (6%)
(b) What’s the write allocate policy? (6%)
(c) If a machine uses the two-level cache architecture, please write the equation of average memory access time for it. (6%)

(3) The protocols to maintain cache coherence for multiple processors are called cache coherence protocols. Key to implementing a cache coherence protocol is tracking the state of any sharing of a data block. There are two classes of protocols, which use different techniques to track the sharing status, i.e., directory based and snooping. Please describe them. (10%)

(4) There are two ways to connect multiple computers, i.e., using shared medium or switched medium. Please use block diagram to illustrate these two ways, and give their advantages and disadvantages. (4/6%)

![Diagram](image)

**Fig. 1**

(5) (15%) Three enhancements with the following speedups are proposed for a new architecture: Speedup1 = 30, speedup2 = 20, Speedup3 = 15. Only one enhancement is usable at a time.

(a) If enhancements 1 and 2 are each usable for 25% of the time, what fraction of the
time must enhancement 3 be used to achieve an overall speedup of 10? (6%)  
(b) Assume, for some benchmark, the possible fraction of use is 15% for each of enhancements 1 and 2 and 70% for enhancement 3. We want to maximize performance. If only one enhancement can be implemented, which should it be? If two enhancements can be implemented, which should be chosen? (9%)  

(6) (15%) Consider adding a new index addressing mode to MIPS. The addressing mode adds two registers and an 11-bit signed offset to get the effective address. Our compiler will be changed so that code sequences of the form

\[
\text{ADD R1, R1, R2} \\
\text{LW Rd, 100(R1)} \quad \text{(or store)}
\]

will be replaced with a load (or store) using the new addressing mode. Suppose that displacement loads and stores constitute 26% and 10%, respectively, of the instruction mix for SPECint2000 programs.

(a) Assume that the new addressing mode can be used for 10% of the displacement loads and stores. What is the ratio of instruction count on the enhanced MIPS compared to the original MIPS? (7%)  
(b) If the new addressing mode lengthens the clock cycle by 5%, which machine will be faster and by how much? (8%)  

(7) (20%) Dynamical scheduling.

(a) Describe the key concepts of Tomasulo’s algorithm. (6%)  
(b) Use the following code sequence, show what the status tables (instruction status, reservation stations, and register status) look like when the MUL.D is ready to write its result. Assume that two load units, three adders and two multipliers are available for use. Division operation is executed in the multiplier. (14%)  

1. L.D   F6, 34(R2)  
2. L.D   F2, 45(R3)  
3. MUL.D F0, F2, F4  
4. SUB.D F8, F2, F6  
5. DIV.D F10, F0, F6  
6. ADD.D F6, F8, F2