1. Consider the following MIPS instruction sequence
   \[
   \text{Lw } $2, 20(\$1) \quad /\$2 \leftarrow \text{memory}[\$1+20] \\
   \text{Add } $4, $2, $5 \quad /\$4 \leftarrow $2+$5
   \]
   The input operand to add, i.e. $2$, depends on the output operand of Lw. If this instruction sequence is executed in a 5-stage pipeline as shown below, the input operand $2$ to add will not be ready from Lw. The execution will be incorrect. The design of the following circuit will stall the pipeline by inserting a pipeline bubble so that the output operand from Lw can be forwarded to add in time.
   (a) Explain how the circuit works to insert a bubble between Lw and Add in the pipeline.
(b) Suppose the circuit does not insert a bubble and let the instruction following the Lw to continue execution, even if they are dependent. Explain how the compiler can do to ensure the correctness of the execution.

(c) Use the diagram below to show where translation-lookaside buffer (TLB) should appear in the pipeline.
2. Suppose the loop in the following program segment will be executed three times and exit to the label Exit. Each instruction is 32-bit long.

```
And $t1, $s3, $s3
Or  $t2, $t1, $s2
Loop:  add $t3, $t2, $s6
       Sub $t0, $s2, $s6
       Bne $t0, $s5, Exit  //go to Exit if $t0 ≠ $s5
       Add $s3, $s3, $s4
       J Loop
Exit:  ...... 
```

Suppose the above code sequence is initially stored in the memory starting at location 00400000\textsubscript{hex}. When it is executed, the instructions are moved to the instruction cache. The instruction cache has 4 blocks in total; each block is 32-bit long. It is organized as a 2-way set associative cache.

(a) Trace the execution of this sequence and mark the instructions that will cause a cache miss. Note that the instructions inside the loop will be executed several times.

(b) For the above misses, identify and specify the instruction that cause compulsory misses and conflict misses.
Note:

1. This is a close book examination. You may use a calculator.

2. There are 5 pages in this exam.

3. Please write down your solution for a question on the same page. You may write on the back of the paper.

4. Show all your work; no points will be given if you show the results only.

5. Good luck!

<table>
<thead>
<tr>
<th>Problem</th>
<th>Points</th>
<th>Score</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>15</td>
<td></td>
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<tr>
<td>2</td>
<td>15</td>
<td></td>
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<tr>
<td>3</td>
<td>20</td>
<td></td>
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<tr>
<td>4</td>
<td></td>
<td></td>
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<tr>
<td>5</td>
<td></td>
<td></td>
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<td>6</td>
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<td>7</td>
<td></td>
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Total 100
1. (15%) Three enhancements with the following speedups are proposed for a new architecture: Speedup1 = 30, Speedup2 = 20, Speedup3 = 15. Only one enhancement is usable at a time.

   (a) If enhancements 1 and 2 are each usable for 25% of the time, what fraction of the time must enhancement 3 be used to achieve an overall speedup of 10? (6%)

   (b) Assume, for some benchmark, the possible fraction of use is 15% for each of enhancements 1 and 2 and 70% for enhancement 3. We want to maximize performance. If only one enhancement can be implemented, which should it be? If two enhancements can be implemented, which should be chosen? (9%)
2. (15%) Consider adding a new index addressing mode to MIPS. The addressing mode adds two registers and an 11-bit signed offset to get the effective address. Our compiler will be changed so that code sequences of the form
   \[
   \text{ADD R1, R1, R2} \\
   \text{LW Rd, 100(R1) (or store)}
   \]
will be replaced with a load (or store) using the new addressing mode. Suppose that displacement loads and stores constitute 26% and 10%, respectively, of the instruction mix for SPECint2000 programs.

   (a) Assume that the new addressing mode can be used for 10% of the displacement loads and stores. What is the ratio of instruction count on the enhanced MIPS compared to the original MIPS? (7%)

   (b) If the new addressing mode lengthens the clock cycle by 5%, which machine will be faster and by how much? (8%)
3. (20%) Dynamical scheduling.
   (a) Describe the key concepts of Tomasulo’s algorithm. (6%)
   (b) Use the following code sequence, show what the status tables (instruction status, reservation stations, and register status) look like when the MUL.D is ready to write its result. Assume that two load units, three adders and two multipliers are available for use. Division operation is executed in the multiplier. (14%)

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</thead>
<tbody>
<tr>
<td>1.</td>
<td>L.D</td>
<td>F6, 34(R2)</td>
</tr>
<tr>
<td>2.</td>
<td>L.D</td>
<td>F2, 45(R3)</td>
</tr>
<tr>
<td>3.</td>
<td>MUL.D</td>
<td>F0, F2, F4</td>
</tr>
<tr>
<td>4.</td>
<td>SUB.D</td>
<td>F8, F2, F6</td>
</tr>
<tr>
<td>5.</td>
<td>DIV.D</td>
<td>F10, F0, F6</td>
</tr>
<tr>
<td>6.</td>
<td>ADD.D</td>
<td>F6, F8, F2</td>
</tr>
</tbody>
</table>